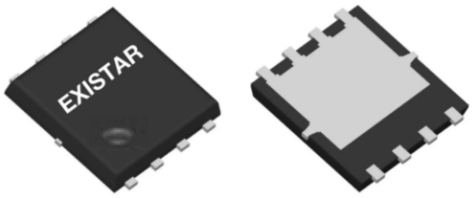
N-Channel 40V MOSFET

E040N3P0HL1

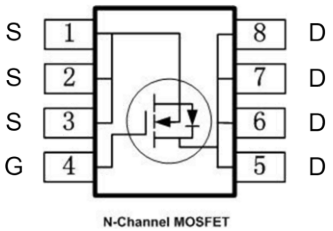
V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
40V	3.0 @ V_{GS} = 10V	110

PDFN5X6



Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested



Pb-free
RoHS COMPLIANT
HALOGEN FREE

Applications

- DC/DC conversion
- Power switch
- PD charger
- Moto driver

Package And Ordering Information

Ordering code	Package	Marking
E040N3P0HL1	PDFN5x6	E040N3P0HL1

Ordering Information

Package	Units/ Reel	Reels/ Inner Box	Units/ Inner Box
PDFN5x6	5000	1	5000

Key Performance Parameters

Parameter	Value	Unit
VDS, min @ Tj(max)	40	V
ID, pulse	430	A
RDS(ON), max @ VGS=10V	3	mΩ
Qg	47	nC

Absolute Maximum Ratings at Tj=25°C Unless Otherwise Noted

Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	±20	
Continuous drain current	T_C=25°C	I_D	110	A
	T_C=100°C		-	
Pulsed drain current		$I_{D,pulse}$	430	
Avalanche energy, single pulse		E_{AS}	45	mJ
Power dissipation	T_C=25°C	P_D	45	W
	T_A=25°C		-	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	3.4	°C/W
Thermal resistance, junction-to-ambient	Steady state	$R_{\theta JA}$	62	

Electrical Characteristics at Tj=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Drain to source breakdown voltage	$V_{(BR)DSS}$	40			V	V_{GS} = 0, I_D = 250 μA
Gate-source threshold voltage	$V_{GS(th)}$	1.2		2.3	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-body leakage	I_{GSS}			±100	nA	V_{DS} = 0 V, V_{GS} = ±20 V
Zero gate voltage drain current	I_{DSS}			1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Drain-source on-resistance	$R_{DS(on)}$		2.2	3	mΩ	V_{GS} = 10 V, I_D = 40 A
Drain-source on-resistance	$R_{DS(on)}$		3.3	4.5	mΩ	V_{GS} = 4.5 V, I_D = 30 A

Forward transconductance	g_{fs}		-		S	V_{DS} = 5 V, I_D = 30 A
Gate resistance	Rg		1.9		Ω	f=1MHz
Gate Charge						
Total gate charge	Qg		47		nC	V_{DS} = 20 V, I_D = 40 A, V_{GS} = 10 V
Gate-source charge	Qgs		7.8			
Gate-drain charge	Qgd		10.6			
Dynamic						
Turn-on delay time	$t_{d(on)}$		8.5		ns	V_{DS} =20 V, I_D =40 A, V_{GS} = 10 V, R_{GEN} = 3 Ω
Rise time	t_r		78			
Turn-off delay time	$t_{d(off)}$		37			
Fall time	t_f		28			
Input capacitance	C_{iss}		2440		pF	V_{DS} =20 V, V_{GS} = 0 V, f = 1MHz
Output capacitance	C_{oss}		820			
Reverse transfer capacitance	C_{rss}		85			
Body Diode						
Diode forward voltage	V_{SD}			1.3	V	V_{GS} = 0 V, I_F = 40 A
Reverse recovery time	t_{rr}		32		ns	V_R= 20 V, I_S =40 A, di/dt = 100 A/μs
Reverse recovery charge	Q_{rr}		16		nC	

Electrical Characteristics Diagrams

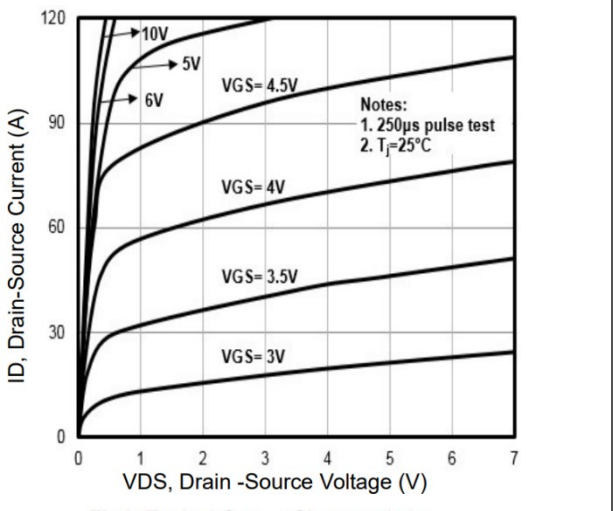


Fig1. Typical Output Characteristics

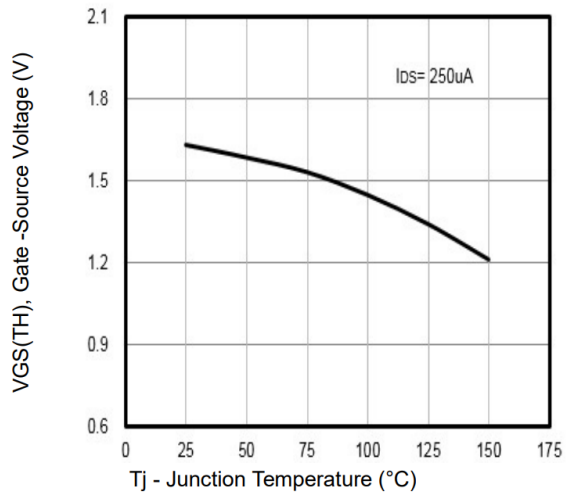


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

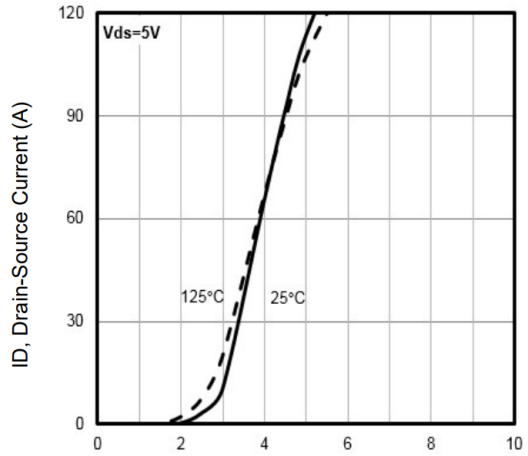


Fig3. Typical Transfer Characteristics

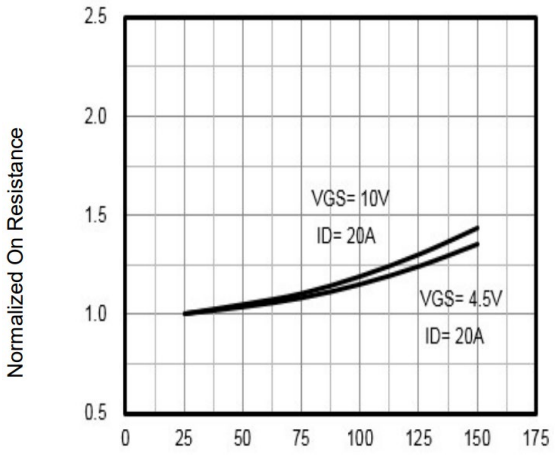


Fig4. Normalized On-Resistance Vs. Tj

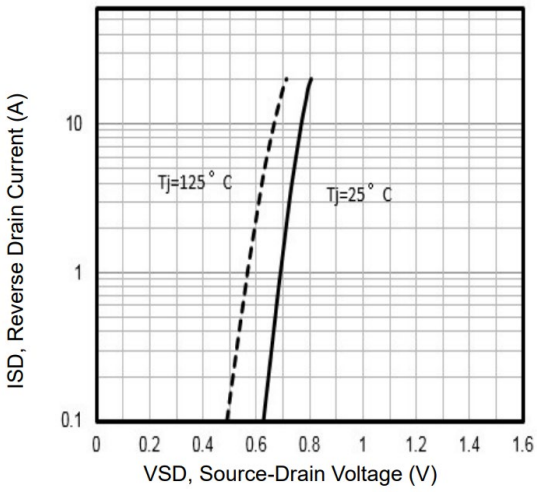


Fig5. Typical Source-Drain Diode Forward Voltage

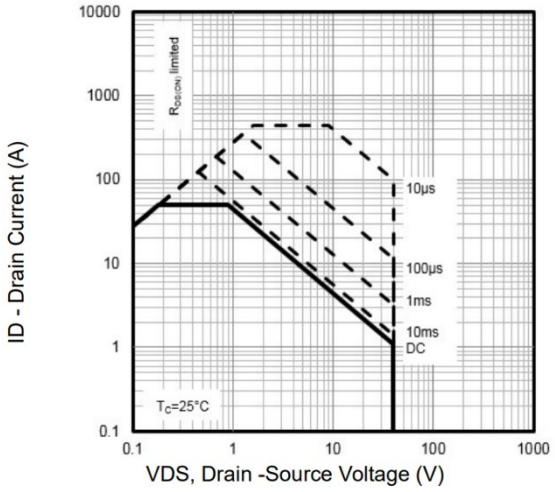


Fig6. Maximum Safe Operating Area

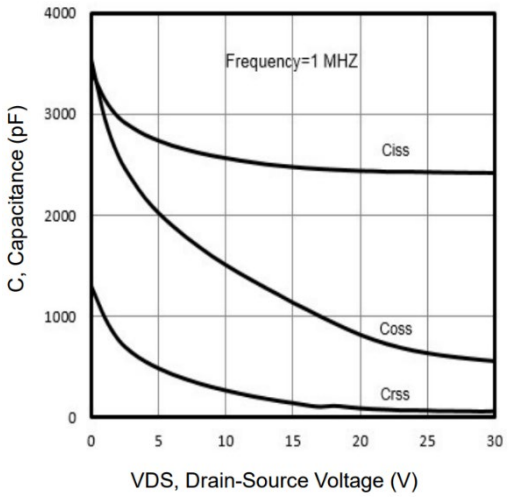


Fig7. Typical Capacitance Vs. Drain-Source Voltage

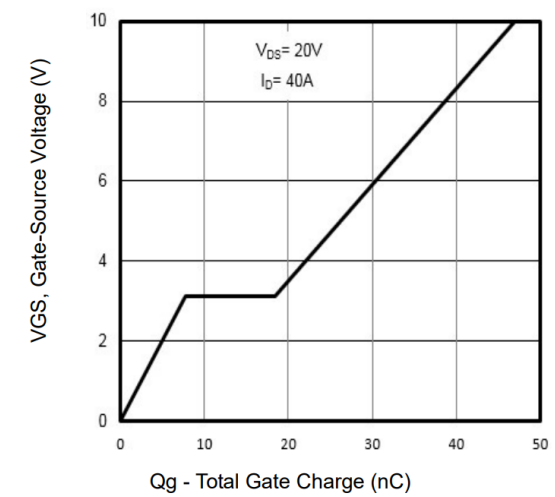


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

Test circuits and waveforms

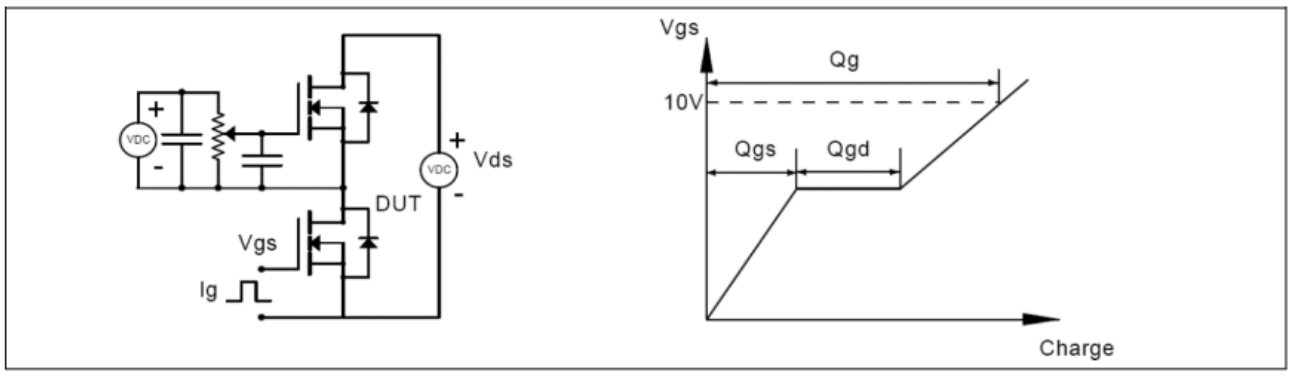


Figure 1. Gate charge test circuit & waveform

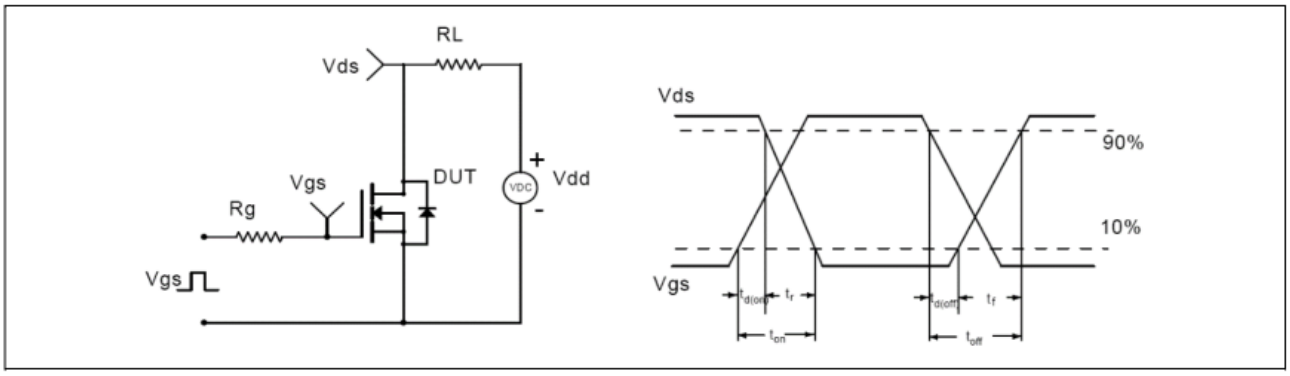


Figure 2. Switching time test circuit & waveforms

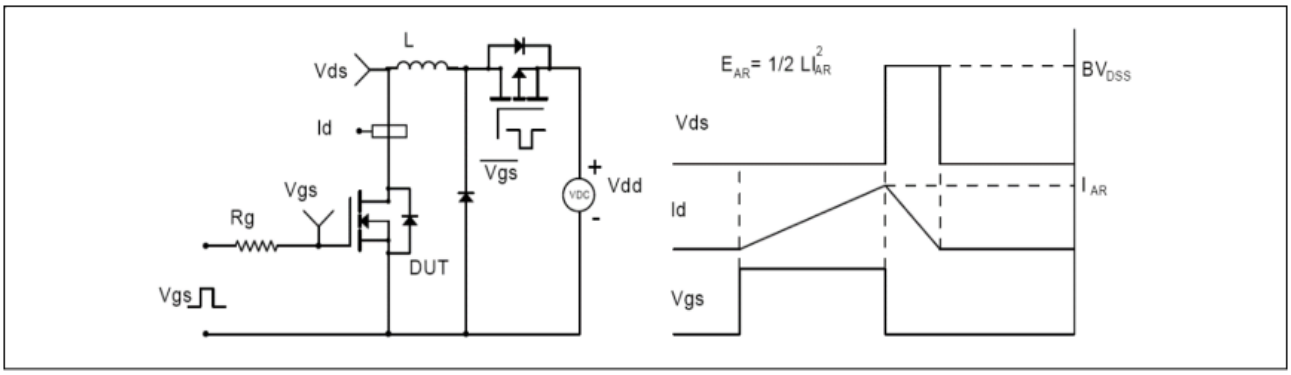


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

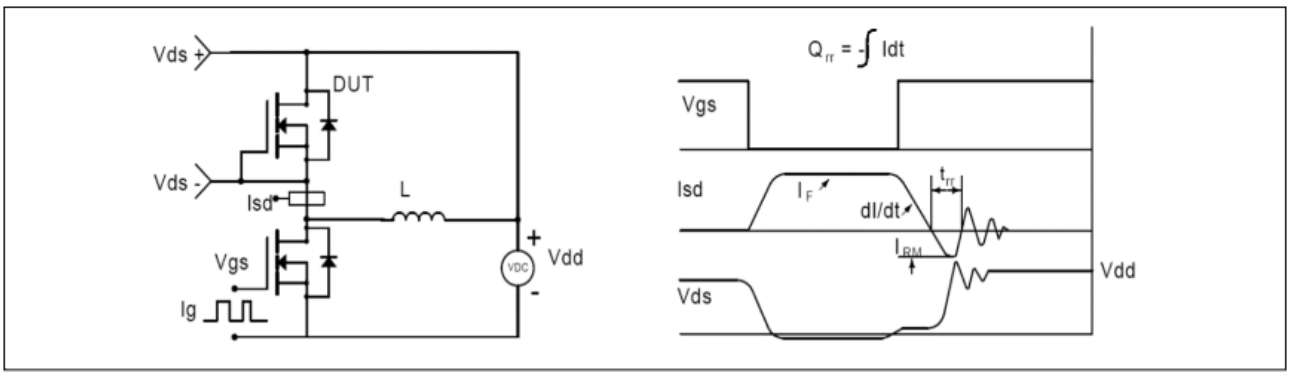
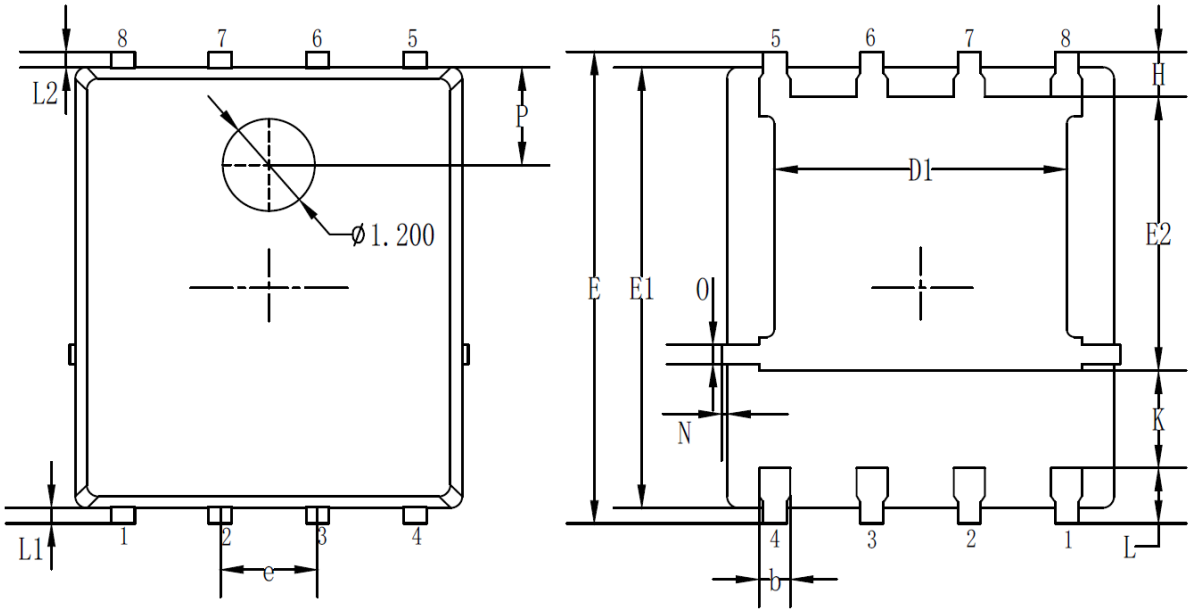
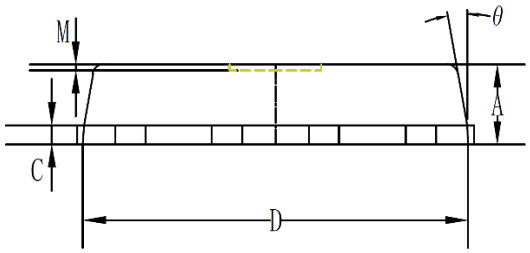


Figure 4. Diode reverse recovery test circuit & waveforms

Package Outline Dimensions





Symbols	Millimeters		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.20
D1	3.72	3.82	3.92
E	0.60	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF.		
θ	8°	10°	12°
M	0.08 REF.		
N	0	-	0.15
O	0.25 REF.		
P	1.28 REF.		

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